REMARKS

In the January 30, 2004 Office Action, the Examiner noted that claims 1-11 were pending and claims 8, 9 and 11 were allowed. In addition, claims 1-6 and 10 were rejected under 35 U.S.C. § 102(e) and claim 7 was rejected under 35 U.S.C. § 103(a). In rejecting the claims U.S. Patent Nos. 6,470,458 B1 to Dreps et al. and 6,552,998 B1 to Matsunaga were cited. Claims 1-11 still remain in the case. The Examiner's rejection is traversed.

The Application

The subject application is directed to a time adjusting system which adjusts the timers of a plurality of processors in a multi-processor system. Specifically, a time synchronous signal is generated and outputted from an output circuit of one of the processors and then inputted to an input circuit of the processor and travels through the time adjusting system and returns to the input circuit of the processor after being propagated through a distributing circuit, and the distributing circuit distributes the time synchronous signal to all of the processors. The travel time is measured and the measured time is used to synchronize timers of the processors.

The Prior Art

U.S. Patent No. 6,470,458 B1 to Dreps et al.

Dreps et al. is directed to self-synchronization of a plurality of chips contained in a data processing system. In particular, a synchronization pattern is transmitted from a secondary chip to a primary chip and then retransmitted to the secondary chip. The secondary chip then logs the number of clock cycles required for the pattern to complete a round trip and compares the number of clock cycles to a predetermined value. The local clock of the secondary chip is then adjusted based upon the comparison result (see column 2, lines 34-42 and column 5, lines 55-59).

U.S. Patent No. 6,552,998 B1 to Matsunaga

Matsunaga is directed to a two-way communication system having a central processing unit which creates a round-trip propagation delay measurement signal and outputs it to a transceiver and a round-trip propagation delay measurement unit. When the central processing unit receives delays of subscriber stations from the round-trip propagation delay measurement unit, it calculates the transmission delays and then outputs them to a storage unit and creates a transmission delay setting signal. The round-trip propagation delay measurement unit measures the interval between the time the transceiver transmits the signal to each of the subscriber

stations and the time the transceiver receives an echo signal and then outputs the result as a roundtrip propagation delay to the central processing unit (see column 13, lines 21-41).

Rejections under 35 U.S.C. § 102

On page 2 of the Office Action, claims 1-6 and 10 were rejected under 35 U.S.C. § 102(e) as being anticipated by Dreps et al. The present claimed invention distinguishes, because unlike Dreps et al., the time synchronous signal does not make a round trip between a pair of processors, instead it is sent out from a processor to a plurality of processors and returns to the input circuit of the originating processor. As mentioned above, in the system taught in Dreps et al., the pattern is sent from a slave chip to a master chip and returned to a slave chip and then the slave chip counts the number of clock cycles required to complete a round trip and adjusts a clock by the difference between the number of clock cycles counted and a predetermined value. Nothing was cited or has been found suggesting

> propagating the time synchronous signal output from the output circuit of one of the processors to all of the processors in the multi-processor system and ... returning the time synchronous signal to the input circuit of the one of the processors after being propagated in the multi-processor system; ... measuring a time during which the one of the processors outputs the time synchronous signal and inputs the time synchronous signal ... [and] using the measured time as a time for distributing the time synchronous signal to the plurality of processors...

(e.g., claim 10, lines 6-16). The only features identified in the Office Action as corresponding to the features recited above in claim 10 were the master and slave chips as recited in column 5, lines 54-59, and primary and secondary chips as recited in column 2, lines 34-42.

Similar limitations to those discussed with respect to claim 10 are recited in claim 1 and claims 2-6 depend from claim 1. Thus, it is submitted that claims 1-6 and 10 patentably distinguish over Dreps et al.

Rejections under 35 U.S.C. § 103

On page 4 of the Office Action, claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Dreps et al. in view of Matsunaga. As mentioned above, Dreps et al. fails to teach or suggest all of the features recited in claim 1 from which claim 7 depends. In addition, nothing was cited or has been found in Matsunaga suggesting a time synchronous signal returning after being propagated through a distributing circuit in a multi-processor system, the distributing circuit distributing the time synchronous signal to all of the processors. Since claim 7 depends from claim 1, it is submitted that claim 7 patentably distinguishes over the

combination of Dreps et al. and Matsunaga for the reasons discussed above with respect to claim 1.

Summary

It is submitted that the cited references fail to teach or suggest all of the features recited in the present claimed invention. Thus, it is submitted that claims 1-6 and 10 are in condition suitable for allowance. Reconsideration of the claims and an Early Notice of Allowance are earnestly solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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